COMPUTING DEVICE 100

MAIN MEMORY 102

MEMORY CONTROLLER 104

COHERENT NETWORK 106

INPUT/OUTPUT DEVICE 118

INPUT/OUTPUT CONTROLLER 114

INPUT/OUTPUT CACHE 116

CACHE CONTROLLER 108

CENTRAL PROCESSING UNIT 112
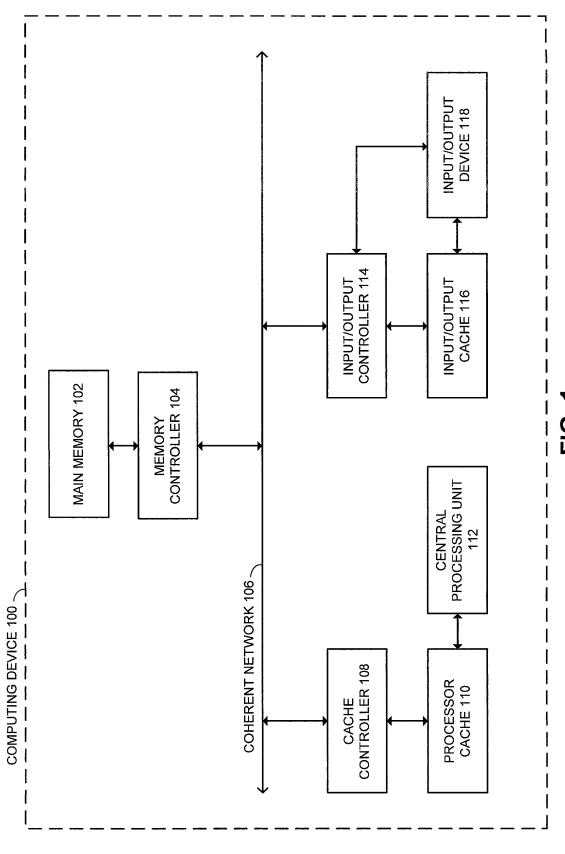
PROCESSOR CACHE 110

FIG. 1

MEMORY CONTROLLER 104

ERROR DETECTION AND CORRECTION 202

READING MECHANISM 204

WRITING MECHANISM 206

MARKING MECHANISM 208

SCRUBBING MECHANISM 210
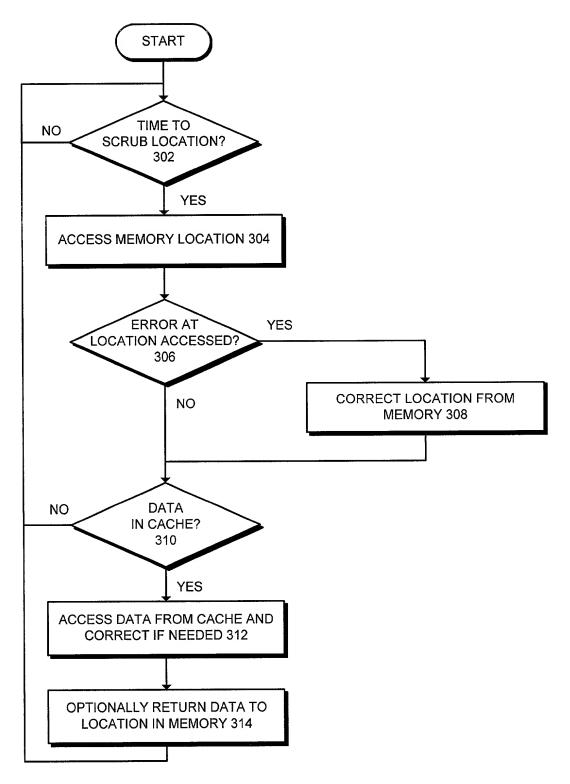
DETECTING MECHANISM 212

FIG. 2

START

TIME TO
SCRUB LOCATION?
302

NO

YES

ACCESS MEMORY LOCATION 304

ERROR AT
LOCATION ACCESSED?
306

YES

NO

CORRECT LOCATION FROM
MEMORY 308

DATA
IN CACHE?
310

NO

YES

ACCESS DATA FROM CACHE AND
CORRECT IF NEEDED 312

OPTIONALLY RETURN DATA TO
LOCATION IN MEMORY 314

FIG. 3